REMARKS

Claims 1, 7, 16, 17, 19-21, 23, 33-36, and 38 are pending. Independent claim 16 stands as previously presented, and claim 1 has been amended to include limitations from claims 2 and 37 (which are cancelled with this response). Therefore, the amendment to claim 1 does not raise a new issue that merits a new search, and entry of this amendment is respectfully requested because it puts the claims in better format for appeal. Claim 38 has also been amended to be consistent with amended claim 1 and does not require a new search. Reconsideration of the application is respectfully requested for at least the following reasons.

I. REJECTION OF CLAIM 1 UNDER 35 U.S.C. § 103(a).

Claim 1 was rejected under §103(a) as obvious over U.S. Pat. No. 6,545,358 (Jeong) in view of U.S. Pat. No. 5,117,276 (Thomas) and further in view of U.S. Pat. No. 5,827,782 (Shih). Claim 1 has been amended to include limitations from claims 2 and 37, which are cancelled with this response. Withdrawal of this rejection is requested for at least the following reasons.

i. The prior art of record does not teach a conductive barrier layer conformal to the vias, where a bottom surface of the conductive barrier layer abuts at least one of the aluminum regions in the uppermost layer; as recited in amended claim 1.

Although Fig. 3 of Jeong teaches an aluminum metal layer 23 and a barrier layer 39, where the barrier layer 39 is conformal to holes 37 in an insulating layer 27; Jeong does not teach a ***bottom surface of the barrier layer that abuts at least one of the aluminum regions***, as recited in amended claim 1. Notably, in Fig. 3 of Jeong, a first plug 51 and a capping layer 25 separate a bottom surface of the barrier layer from the aluminum metal layer 23. Also, in Fig. 2 of Jeong, a first plug 33 separates a bottom surface of the barrier layer from the aluminum metal layer 23.

There is no teaching or suggestion in Jeong to modify the reference to arrive at present claim 1. Moreover, one of ordinary skill would not remove the first plug (51 or

33) or the capping layer 25 of Jeong, because such a modification would render Jeong inoperable and/or unsuitable for its intended purpose. More specifically, the first plug 33 in Jeong is necessary because it is "less like to separate or detach from the recess 29 in a planarization process used to form the first plug 33." *See* Col. 3, lines 26-30.

Therefore, because the prior art of record does not teach or suggest all limitations of claim 1, withdrawal of this rejection is respectfully requested.

II. REJECTION OF CLAIMS 16 UNDER 35 U.S.C. § 103(a).

Claim 16 was rejected under §103(a) as being obvious over U.S. Pat. No. 6,545,358 (Jeong) in view of U.S. Pat. No. 6,218,282 (Buynoski), and further in view of U.S. Pat. No. 5,827,782 (Shih). Withdrawal of this rejection is requested for at least the following reason.

i. The prior art of record does not teach an uppermost layer comprising bond pads, wherein multiple vias are formed over individual bond pads as recited in claim 16.

In the cited art, the only feature that is described as a "bond pad" is reference numeral 41 in Buynoski (*see* Buynoski Fig. 4, col. 5, lines 65-67). Notably, ***this bond pad 41 is at an exposed surface on the structure, and therefore does not include multiple vias formed over it as required in claim 16.*** Although the pending OA asserts that several other features in the prior art are bond pads, as will be appreciated by a person of ordinary skill in the art and as set forth below, ***these other features are not bond pads***. Therefore, the prior art of record fails to multiple vias formed over individual bond pads as recited in claim 16, and withdrawal of the §103 rejection is respectfully requested.

First of all, the pending OA asserts that Fig. 4 of Jeong teaches bond pads 23. Pending OA, p. 4, item 11. However, the applicants respectfully disagree. The lower metal layer 23 is not called out as a "bond pad" anywhere in Jeong's specification. As one of ordinary skill in the art appreciates, bond pads are typically an area on the chip to which external electrical connections can be bonded. Therefore, because Jeong

does not describe lower metal layer 23 as a bond pad, and because the lower metal layer 23 appears to be un-exposed to the environment outside the integrated circuit (i.e., making it *inaccessible* to an external electrical connection), ***lower metal layer 23 does not constitute a bond pad***. Even if Jeong did teach a bond pad, the pending OA admits that Jeong fails to teach multiple vias formed over individual bond pads.

To remedy this admitted defect in Jeong, the pending OA cites Buynoski and states that "Buynoski (e.g., fig. 4) shows an integrated circuit having multiple vias 1 formed over individual bond pads (metal 1)." However, Buynoski does not state that the metal 1 layer is a bond pad, but rather calls out element 41 as a bond pad. (*See*, col. 5, lns. 65-66). One skilled in the art would recognize that the structures below element 41 (metal 1 – metal 5 and via 1 – via 5) are lower levels within the metal stack ***and are not part of the bond pad 41***. In particular, the dense via structure of Buynoski points to the fact that Buynoski intended these lower metal and via levels to be support levels to the bonding pad 41, not the bonding pad itself. (See, e.g., figure 1).

Further, one skilled in the art would recognize that Buynoski's metal 1 layer is not a bond pad for several additional reasons. For example, metal 1 generally consists of thin lines used for local interconnect between closely spaced device features (e.g., source/drain regions). Bond pads, by contrast, require an area that is sufficiently large for physically bonding an external electrical connection to the integrated circuit. Because integrated circuit manufacturers want to maximize the density of device features per unit area, one of ordinary skill in the art would not insert a bond pad in place of Buynoski's metal 1 layer, because doing so would force the devices under the bond pad to have a much lower density per unit area, thereby significantly raising the cost-point of the integrated circuit.

Therefore, because the prior art of record does not teach or suggest all limitations of claim 16, withdrawal of this rejection is respectfully requested.

III. CONCLUSION

For at least the above reasons, independent claims 1 and 16 and all claims depending either directly or indirectly therefrom are believed to be in condition for allowance and notice thereof is requested.

Should the Examiner feel that a telephone interview would be helpful to facilitate favorable prosecution of the above-identified application, the Examiner is invited to contact the undersigned at the telephone number provided below.

In addition, should any fees be due as a result of the filing of this response, the Commissioner is hereby authorized to charge the Deposit Account Number 20-0668, TI-36853.

Respectfully submitted,
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